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10/549,642	09/20/2005	Pierre Hermanus Woerlee	NL 030332	8061
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PHILIPS INTELLECTUAL PROPERTY & STANDARDS			SASINOWSKI, ANDREW	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/549,642	<b>Applicant(s)</b> WOERLEE ET AL.
	<b>Examiner</b> ANDREW J. SASINOWSKI	<b>Art Unit</b> 4163

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 20 September 2005.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-9 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 20 September 2005 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-166/08)  
 Paper No(s)/Mail Date 7/31/2007

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_

5) Notice of Informal Patent Application

6) Other: \_\_\_\_\_

**DETAILED ACTION*****Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 through 3, 6, and 8 through 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura et. al. [WO 01/54119].
3. Regarding claim 1, Nakamura teaches a record carrier of a writable type [pg. 1, lines 8-12, note that record carriers of the optical type inherently use the same laser for recording or reproducing data, the only difference being beam power] for recording information by writing marks in a track via a beam of radiation [pg. 1, 8-12] entering through an entrance face of the record carrier [fig.8, items 801 and 805], the marks being recorded in recording units representing addressable blocks of information [pg. 2, lines 11-20, note that while this element is mentioned as prior art, it is inherent to optical record carriers], the record carrier comprising at least a first recording layer and a second recording layer [pg. 6, lines 9-10], the first recording layer being present at a position closer to the entrance face than the second recording layer [pg. 6, lines 9-10, note that one layer is inherently closer to the entrance face than the other layer], each recording layer comprising a pre-formed recording control pattern for indicating the track [claim 24], the pattern comprising physical addresses [claim 24] having

a predefined number of address bits [pg. 2, lines 11-20] that indicate the physical position of the physical address with respect to a starting point of the track [pg. 16, lines 8-13], and at least one address bit of said predefined number of address bits of the physical address constituting at least one layer address bit that has a value indicating the recording layer [pg. 6, 9-16].

4. Regarding claim 2, Nakamura teaches a record carrier as claimed in claim 1 [see above], wherein the at least one layer address bit corresponds to the most significant bit of the physical address [pg. 6, 9-16].

5. Regarding claim 3, Nakamura teaches a record carrier as claimed in claim 1 [see above], wherein the layer address bit has the value zero in the first recording layer [fig. 11b].

6. Regarding claim 6, Nakamura teaches all of the record carrier elements as discussed in claim 1. Furthermore, Nakamura teaches a device for recording marks in a track on a record carrier via a beam of radiation [pg. 1, 8-12], the device comprising a head for providing the beam [fig. 8, item 813], recording means for writing marks in the track via the beam [pg. 1, 8-12], the marks being recorded in recording units representing addressable blocks of information [pg. 2, 11-20], a front-end unit for generating a scanning signal for detecting marks in the track [claim 25], and demodulation means for retrieving the physical addresses including the at least one layer address bit from the pre-formed recording control pattern [fig. 8, item 812], and a layer unit for detecting a recording layer in dependence of the at least one layer address bit [fig. 8, item 812].

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7. Regarding claim 8, Nakamura teaches the device as claimed in claim 6.
8. Furthermore, Nakamura teaches a device wherein the recording means are arranged for recording the units representing addressable blocks of information including a logical address field [pg. 2, lines 11-20], the logical address field containing a logical address value based on the physical address and the at least one layer address bit [claim 24], in particular the logical address field containing a copy of the predefined number of address bits including the at least one layer address bit [claim 24].
9. Regarding claim 9, Nakamura teaches device as claimed in claim 6 [see above], wherein the layer unit is arranged for interrupting a recording process in dependence on a deviation of an intended recording layer value and a layer value detected from the at least one layer address bit [pg. 42, lines 1-10, note that "addressing such situations" inherently implies a cancellation of the current recording process].

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 4 through 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Lee et. al. [US 2002/0176346].

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12. Nakamura teaches a record carrier as claimed in claim 1 [see above], wherein the pre-formed recording control pattern is constituted by a pregroove [fig. #1, item 101] indicating the position of the track [pg. 9, lines 10-15], the pregroove exhibiting a wobble constituted by displacements of the pregroove in a direction transverse to the longitudinal direction of the track [fig. #1, item 101].

13. However, Nakamura does not teach a record carrier featuring a wobble exhibiting a modulation representing the physical addresses including the at least one layer address bit.

14. Lee teaches a record carrier featuring a wobble exhibiting a modulation representing the physical addresses including the at least one layer address bit [0008].

15. It would have been obvious at the time of invention to one of ordinary skill in the art to combine the wobble modulation taught by Lee with the record carrier taught by Nakamura because combining the two items would provide a predictable result, namely that the wobble modulation featured on the disc would represent physical addresses.

16. Regarding claim 5, Nakamura in view of Lee teach the record carrier as claimed in claim 4.

17. Furthermore, Nakamura teaches a record carrier where the layer address bit has the value one on the second recording layer [fig. 11a].

18. However, Nakamura does not teach a record carrier wherein the pregroove on the first recording layer extends spirally in a first direction and the pregroove on the second recording layer extends spirally in a second direction

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opposite to the first direction for constituting a multi-part recording area interrupted by an intermediate zone that physically is constituted by a first intermediate part located at the end of the first recording layer and a second intermediate part located at the start of the second recording layer.

19. Lee teaches a record carrier wherein the pregroove on the first recording layer extends spirally in a first direction and the pregroove on the second recording layer extends spirally in a second direction opposite to the first direction [0017] for constituting a multi-part recording area interrupted by an intermediate zone [fig. 2c, note that while this element is listed under prior art, it is inherently an efficient way to align two adjacent layers] that physically is constituted by a first intermediate part [fig. 2c] located at the end of the first recording layer and a second intermediate part [fig. 2c] located at the start of the second recording layer.

20. It would have been obvious at the time of invention to one of ordinary skill in the art to combine the multi-layer track structure taught by Lee with the record carrier taught by Nakamura because doing so would have a predictable result, namely that during reproduction of the record carrier the laser beam would not have to jump from the outside radius of the carrier to the inside radius when switching from the first layer to the second layer.

21. Regarding claim 7, Nakamura teaches the device as claimed in claim 6.

22. Furthermore, Nakamura teaches a device wherein the recording means are arranged for recording the units representing addressable blocks of information including a logical address field [pg. 2, lines 11-20], the logical

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address field containing a logical address value based on the physical address [claim 24].

23. However, Nakamura does not teach a device wherein the logical address field differs from the physical address by excluding the at least one layer address bit.

24. Lee teaches a device wherein the logical address field differs from the physical address by excluding the at least one layer address bit [0059, note that the address information does not include layer data but the layer data is conveyed through a predetermined address value pattern, see also fig.3a through fig. 8c].

25. It would have been obvious to one with ordinary skill in the art at the time of invention to combine the address value that excludes the layer address bit with the device taught by Nakamura because doing so would provide a predictable result, namely that less data space would have to be used on the record carrier for identifying the layer of the carrier.

### ***Conclusion***

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Morizumi et. al [US 6,614,736] teaches an optical disc drive and recording/reproducing method with a plurality of similar elements to those present in the present case.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDREW J. SASINOWSKI whose telephone

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number is (571)270-5883. The examiner can normally be reached on Monday to Friday, 7:30 to 5:00, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Robinson can be reached on (571)272-2319. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AJS

/Mark A. Robinson/  
Supervisory Patent Examiner, Art Unit 4163